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09/580,632	05/30/2000	Sven Mattisson	040071-134	1997

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EXAMINER

ODOM, CURTIS B

ART UNIT PAPER NUMBER

2634

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12

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/580,632

Applicant(s)

MATTISSON ET AL.

Examiner

Curtis B. Odom

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3-8, 13, and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shurboff (previously cited in Office Action 7/30/03).

Regarding claim 1, Shurboff discloses a phase detector (Fig. 5) comprising:

a first input (Fig. 5, element 528, column 4, lines 59-64) receives a first signal;

a second input (Fig. 5, element 530, column 4, lines 59-64) that receives a second signal;

a comparison circuit (Fig. 5, column 4, lines 46-58) that generates an output signal that is a function of a phase difference between the first signal and the second signal; and

an operating point circuit (Fig. 5, column 2, lines 45-54, column 4, lines 50-67 and column 5, lines 1-3) that maintains an operating point of the phase detector such that for a predetermined range of both positive and negative phase differences between the first and second signals, the output signal is generated as a substantially linear function of the phase difference between the first signal and the second signal.

Shurboff does not specifically disclose the substantial linearity of the output signal is due at least in part to a shifting of the operating point so that a nonzero output signal corresponds to a nonzero phase difference between the first and second signals. However, the operating circuit of the claimed invention solves the problem of charge-pump asymmetry by shifting the operating point of the phase detector. The operating point the phase detector is shifted by adding unequal delay circuits in the reset path of the phase detector (pg. 11, line 3-pg. 12, line 14, Figs. 12a-12c). Shurboff does disclose solving the problem of charge pump asymmetry in a phase detector by equalizing the amounts of charge from the charge pumps by adding unequal delay circuits in the reset path of the phase detector (column 2, lines 45-54). This operation also linearizes the phase detector (column 2, lines 45-47). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that since shifting the operating point of the phase detector is simply shifting the phase detector from operating in a non-linear region to a linear region that the linearizing operation as taught by Shurboff (column 2, lines 45-54) is equivalent to shifting the operating point of the phase detector. Thus, claim 1 does not constitute patentability.

Regarding claim 3, which inherits the limitations of claim 1, Shurboff discloses the output signal is an output current signal (Fig. 5, element 536); and

the comparison circuit comprises:

a first circuit (Fig. 5, block 502, column 4, lines 4-30 and 59-67) and column 5, lines 1-3) that asserts a first charge pump control signal in response to an edge of the first signal;

Art Unit: 2634

a second circuit (Fig. 5, block 504, column 4, lines 4-30 and 59-67) and column 5, lines 1-3) that asserts a second charge pump control signal in response to an edge of the second signal;

a first charge pump (Fig. 5, block 506, column 4, lines 4-30 and 59-67) that contributes a positive current to the output current in response to assertion of the first charge pump control signal;

a second charge pump (Fig. 5, block 508, column 4, lines 4-30 and 59-67) that contributes a negative current to the output current in response to assertion of the second charge pump control signal;

reset logic (Fig. 5, elements 510, 512, and 514, column 5, lines 4-23) that supplies a reset signal to each of the first and second circuits in response to both of the first and second charge pump control signals being asserted, and

wherein the operating point circuit comprises:

a delay circuit (Fig. 5, block 512, column 5, lines 4-30) that delays at least one of the first and second charge pump control signals from being supplied to the reset logic, wherein a length of time that it takes the first charge pump control signal to be supplied to the reset logic is not equal to the length of time that it takes the second charge pump control signal to be supplied to the reset logic.

Regarding claim 4, which inherits the limitations of claim 3, Shurboff discloses the delay circuit delays only one of the first and second charge pump signals from being supplied to the reset logic (column 5, lines 4-30).

Regarding claim 5, which inherits the limitations of claim 3, Shurboff does not disclose the delay circuit delays both the first and second charge pump signals from

Art Unit: 2634

being supplied to the reset logic. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a second delay could have been implemented in the same manner as the first delay of Fig. 5 to delay the second charge pump signal. Fig. 1 of Shurboff illustrates a second delay (block 112) for a second charge pumps signal. Thus, the delay circuit delaying both the first and second charge pump signals from being supplied to the reset logic does not constitute patentability.

Regarding claims 6-8, Shurboff discloses all the limitations of claims 6-8 (see rejection of claim 3-5 except the use of voltage control signals and voltage generators which use voltage to control the phase detector instead of current as taught by Shurboff. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that it is conventional to use voltage to control a phase detector (Ranger, U.S. Patent No. 4, 818, 950). It would have also been obvious that voltage could have been used to control the phase detector of Shurboff using the same basic components (instead of a charge pump which generates current, there would be a voltage generator which generates voltage, etc) without not having to redesign the circuit. Thus the use of voltage in the phase detector is deemed a design choice and does not constitute patentability.

Regarding claim 13, the claimed method including features that correspond with subject matter mentioned above in the rejection of claim 1 is applicable hereto.

Regarding claim 15, Shurboff discloses all the subject matter of 15 (see rejection of claim 1) including deactivating (column 5, lines 4-30) the first and second charge

Art Unit: 2634

pump control signals in response to both of the first and second charge pump control signals being asserted, and

wherein the step of maintaining the operating point of the phase detector comprises:

delaying (column 5, lines 4-30) at least one of the first and second charge pump control signals from affecting the deactivating step, wherein a length of time that it takes the first charge pump control signal to affect the deactivating step is not equal to the length of time that it takes the second charge pump control signal to affect the deactivating step.

Regarding claim 16, which inherits the limitations of claim 15, Shurboff discloses the delay circuit delays only one of the first and second charge pump signals from affecting the deactivating step (column 5, lines 4-30).

Regarding claim 17, which inherits the limitations of claim 15, Shurboff does not disclose the delay circuit delays both the first and second charge pump signals from affecting the deactivating step. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a second delay could have been implemented in the same manner as the first delay of Fig. 5 to delay the second charge pump signal. Fig. 1 of Shurboff illustrates a second delay (block 112) for a second charge pumps signal. Thus, the delay circuit delaying both the first and second charge pump signals from affecting the deactivating step does not constitute patentability.

Regarding claims 18-20, Regarding claims 6-8, Shurboff discloses all the limitations of claims 18-20 (see rejection of claims 15-17) except the use of voltage control signals and voltage generators which use voltage to control the phase detector

Art Unit: 2634

instead of current as taught by Shurboff. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that it is conventional to use voltage to control a phase detector (Ranger, U.S. Patent No. 4, 818, 950). It would have also been obvious that voltage could have been used to control the phase detector of Shurboff using the same basic components (instead of a charge pump which generates current, there would be a voltage generator which generates voltage, etc) without not having to redesign the circuit. Thus the use of voltage in the phase detector is deemed a design choice and does not constitute patentability.

3. Claims 2, 9-12, 14, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shurboff (cited in Office Action 7/30/03) in view of Turner (IBM Technical Disclosure Bulletin cited in Office Action 7/30/03).

Regarding claim 2, which inherits the limitations of claim 1, Shurboff discloses the phase detector is employed in a PLL, whereby an output frequency of the PLL is a function of the output signal of the phase detector (Fig. 11, column 7, lines 61-64). Shurboff does not disclose the operating point circuit leaks a predefined portion of the output signal so as to prevent the leaked output signal from influencing the output frequency of the PLL.

However, Turner discloses leaking a portion of the output signal in a PLL so as to adjust the PLL to prevent the leaked output signal from influencing the PLL (pgs. 2080-2081). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the operating point circuit of Shurboff with the teachings of Turner in order to all the PLL to adjust the phase difference between the two signals precisely to overcome production tolerances of the circuit.

Art Unit: 2634

Regarding claim 9, Shurboff discloses a PLL (Fig. 11) comprising
a phase detector (Fig. 11, block 500) that comprises:
a first input (column 7, lines 50-52) that receives a reference clock signal;
a second input (column 7, lines 50-52) that receives a feedback signal; and
a comparison circuit (Fig. 11, block 500, column 7, lines 52-55) that generates an
output signal that is a function of a phase difference between the reference clock signal
and the feedback signal;

an operating point circuit (Fig. 5, column 2, lines 45-54, column 4, lines 50-67
and column 5, lines 1-3) that maintains an operating point of the phase detector such that
for a predetermined range of both positive and negative phase differences between the
reference clock and feedback signals, the output signal is generated as a substantially
linear function of the phase difference between the reference clock and the feedback
signals;

a loop filter (Fig. 11, block 1102, column 7, lines 57-59) that generates a PLL
output from the phase detector output signal;

a circuit (Fig. 11, block 1104, column 7, lines 59-61) that generates a PLL output
signal that has a frequency that is controlled by the frequency control signal; and

a frequency divider (Fig. 11, block 1106, column 7, lines 61-64) that generates the
feedback signal from the PLL output signal.

Shurboff does not specifically disclose the substantial linearity of the output
signal is due at least in part to a shifting of the operating point so that a nonzero output
signal corresponds to a nonzero phase difference between the reference clock and the
feedback signals. However, the operating circuit of the claimed invention solves the

Art Unit: 2634

problem of charge-pump asymmetry by shifting the operating point of the phase detector. The operating point the phase detector is shifted by adding unequal delay circuits in the reset path of the phase detector (pg. 11, line 3-pg. 12, line 14, Figs. 12a-12c). Shurboff does disclose solving the problem of charge pump asymmetry in a phase detector by equalizing the amounts of charge from the charge pumps by adding unequal delay circuits in the reset path of the phase detector (column 2, lines 45-54). This operation also linearizes the phase detector (column 2, lines 45-47). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that since shifting the operating point of the phase detector is simply shifting the phase detector from operating in a non-linear region to a linear region that the linearizing operation as taught by Shurboff (column 2, lines 45-54) is equivalent to shifting the operating point of the phase detector.

Shurboff also does not disclose one or more elements that leak a predefined portion of at least one of the phase detector output signal and the frequency control signal so as to prevent the leaked output signal from influencing the output frequency of the PLL.

However, Turner discloses leaking a portion of the output signal in a PLL so as to adjust the PLL to prevent the leaked output signal from influencing the PLL (pgs. 2080-2081). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the operating point circuit of Shurboff with the teachings of Turner in order to all the PLL to adjust the phase difference between the two signals precisely to overcome production tolerances of the circuit.

Art Unit: 2634

Regarding claim 10, which inherits the limitations of claim 9, Turner further discloses that the one or more circuit elements that leak a predefined portion of at least one of the phase detector output signal and the frequency control signal comprise:

one or more circuit elements in the loop filter that leak a predefined portion of the phase detector output signal (pg. 2081) wherein the circuit element which produces the leakage is implemented in the filter to charge the filter.

Regarding claim 11, which inherits the limitations of claim 9, Shurboff further discloses the circuit (Fig. 11, block 1104, column 7, lines 59-61) that generates a PLL output signal that is controlled by the frequency control signal is a VCO.

Regarding claim 12, which inherits the limitations of claim 9, Shurboff does not disclose the circuit that generates a PLL output signal that is controlled by the frequency control signal is a current controlled oscillator. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a current controlled oscillator could have been implemented to perform the same function as the VCO if current was being used to control the PLL. Thus, using a current controlled oscillator is deemed a design choice and does not constitute patentability

Regarding claim 14, which inherits the limitations of claim 13, the claimed method including features that correspond with subject matter mentioned above in the rejection of claim 2 is applicable hereto.

Regarding claims 21 and 22, the claimed method including features that correspond with subject matter mentioned above in the rejection of claims 9 and 10 are applicable hereto.

Art Unit: 2634


Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 703-305-4097. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Curtis Odom
July 8, 2004



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